REMARKS

Present Status of the Application

The drawings are objected to as failing to comply with 37 C.F.R. 1.84(p)(5) because they include the reference characters not mentioned in the description. The disclosure is objected to because of some informalities. Claims 1 and 17 are objected to because of some informalities.

Claims 17-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. Furthermore, claims 1-4, 17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly to point out and distinctly claim the subject matter which Applicants regard as the invention.

Claims 1-4, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shelton et al. (US 6,046,709 A, hereinafter "Shelton"). Claims 1-4, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton in view of Applicants' Admitted Prior Art (hereinafter "AAPA").

In response thereto, Applicants have amended claims 1-4, 17, and 18 to overcome the objections and rejections. Furthermore, FIGs. 3-4 and the disclosures are also amended to overcome the objections. Reconsideration and allowance of the application and presently pending claims 1-4 and 17-18 are respectfully requested.

Discussion for Amendments to Specification

Applicants have corrected some typos in paragraphs [0008] and [0009]. The term "CUP" is corrected to "CPU", and the term "techniques is" is corrected as "techniques are". Paragraph [0023] is also amended to make the abbreviation "DD" clearer and more definite. Specifically, the abbreviation "DD" refers to "Display Device". It is believed that no new matter is added by these amendments to the specification.

Discussion for Amendments to Drawings

The reference characters "32", "33", "35", "36", "37", "39", and "40" in FIG. 3 are cancelled, and the reference characters "37", "39", "40", "42", "43", "45", and "50" in FIG. 4 are cancelled. It is believed that no new matter is added by these amendments to the drawings.

Discussion for Objection to Claims

In claims 1 and 17, the term "an non-responding period" is corrected to be "a non-responding period", and the informalities in claims 1 and 17 are corrected.

Discussion for 35 U.S.C. 112 Rejections of Claims

Claims 17-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement.

Examiner states that the claimed subject matter of "self-adjusting CPU frequency" is not described in the specification. In response thereto, claim 17 is amended to the following:

"A graphics display method for continuously displaying a plurality of graphics data on

multiple display devices of a computer system that contains a central processing unit (CPU) which has a memory controller inside, a graphics-processing unit coupled to the memory controller, and a system memory directly accessed by the CPU, wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and using the common clock source to synchronize blank periods of the display devices;

receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process **to make the CPU self-adjust a CPU clock rate and a power level of the CPU during a non-responding period of the CPU**, wherein memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU; and

executing the power saving process within a least common multiple occurrence of the blank periods of the display devices." **(Emphasis Added)**

In paragraph [0009] in the specification, it states, "a mechanism that detects the power consumption level of an application several times every second and self-adjusts the CPU clock rate and power supply level to reduce power consumption is built into a computer." To reduce the power, the CPU self-adjusts the CPU clock rate. After claim 17 is amended, the rejections under 35 U.S.C. 112, first paragraph, are overcome, and it is believed that no new matter is added by these amendments.

Claims 1-4, 17, and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly to point out and distinctly claim the subject matter which

applicant regard as the invention.

In response thereto, claim 1 is now recited as:

"A graphics display method for continuously displaying **a plurality of graphics data** on multiple display devices of **a computer system** that contains a **central processing unit (CPU)** which has a memory controller inside, a graphics-processing unit coupled to the memory controller, and a system memory directly accessed by the CPU, wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and using the common clock source to synchronize a plurality of blank periods of the display devices;

receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process by the CPU during a non-responding period of the CPU, so as to reduce power consumption of the CPU, wherein memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU; and

executing the power saving process within **a least common multiple occurrence of the blank periods of the display devices." (Emphasis Added)**

In amended claim 1, it is clear that a plurality of graphics data are continuously displayed on multiple display devices of a computer system, and a system memory is included in the computer system. The CPU is the central processing unit. The power saving means reducing power consumption of the CPU after the power saving process is executed, and in the power saving process, the CPU clock rate is self-adjusted by the CPU, or the power level of the CPU is reduced. The non-responding period is the non-responding period of the CPU. The common

clock source is a common clock source that is provided to the multiple display devices. The power saving signal is used to indicate that the power saving process is to be executed, and thus after the power saving signal is received from the CPU, the power saving process is executed within a least common multiple occurrence of the blank periods of the display devices.

After claim 1 is amended, it is believed that the rejections under 35 U.S.C. 112, second paragraph are overcome. All amendments to claim 1 are supported by the specification of the present invention, and it is believed that no new matter is added.

In response thereto, claim 2 is now amended to the following:

"2. The method of claim 1, further comprising a step of detecting the upcoming least common multiple occurrence of the blank periods of the display devices **before executing the power saving process." (Emphasis Added)**

The "step" is the step of executing the power saving process. After claim 2 is amended, it is believed that the rejections under 35 U.S.C. 112, second paragraph are overcome. The amendments to claim 2 are supported by the specification of the present invention, and it is believed that no new matter is added.

In response thereto, claims 3 and 4 are now amended to the following:

"3. The method of claim 1, wherein **the blank periods can be a plurality of horizontal blank periods (HBPs) or a plurality of vertical blank periods (VBPs).**"; and

"4. The method of claim 3, wherein **the horizontal blank periods or the vertical blank periods are provided by the graphics-processing unit." (Emphasis Added)**

The term "blank period" should be "blank periods", and the terms "horizontal blank period" and "vertical blank period" should be "horizontal blank periods" and "vertical blank periods",

respectively. After claims 3 and 4 are amended, it is believed that the rejections under 35 U.S.C. 112, second paragraph are overcome. The amendments to claims 3 and 4 are supported by the specification of the present invention, and it is believed that no new matter is added.

In response thereto, claim 17 is recited as:

"17. A graphics display method for continuously displaying **a plurality of graphics data** on multiple display devices of **a computer system** that contains a central processing unit (CPU) which has a memory controller inside, a graphics-processing unit coupled to the memory controller, and a **system memory** directly accessed by the CPU, wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and using the common clock source to synchronize blank periods of the display devices;

receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process to make the CPU self-adjust a CPU clock rate and a power level of the CPU during a non-responding period of the CPU, wherein memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU; and

executing the power saving process within a least common multiple occurrence of the blank periods of the display devices." (Emphasis Added)

Regarding claim 17, the reasons by which the rejections under 35 U.S.C. 112, second paragraph are overcome are the same as those in claim 1. After claim 17 is amended, it is believed that the rejections under 35 U.S.C. 112, second paragraph are overcome. All amendments to claim 17 are supported by the specification of the present invention, and it is

believed that no new matter is added.

Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being dependent upon rejected base claim 17. Since claim 17 is amended to overcome the rejections under 35 U.S.C. 112, second paragraph, claim 18 should no longer be rejected under 35 U.S.C. 112, second paragraph.

Discussion for 35 U.S.C. 102 Rejections to Claims

Claims 1-4, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shelton.

Examiner fails to provide the reasons as to why claims 1-4, 17, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Shelton. **The features and limitations in claims 1-4, 17, and 18 should be compared with Shelton when Examiner rejected claims 1-4, 17, and 18 under 35 U.S.C. 102(b) as being anticipated by Shelton.**

Discussion for 35 U.S.C. 103 Rejections to Claims

Claims 1-4, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shelton in view of AAPA.

Regarding claim 1, claim 1 is now recited as:

"A graphics display method for continuously displaying a plurality of graphics data on multiple display devices of a computer system that contains a central processing unit (CPU) which has a memory controller inside, a graphics-processing unit coupled to the memory controller, and **a system memory directly accessed by the CPU**, wherein the display devices

are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and using the common clock source to synchronize blank periods of the display devices;

receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process to make the CPU self-adjust a CPU clock rate and a power level of the CPU during a non-responding period of the CPU, wherein memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU; and

executing the power saving process within a least common multiple occurrence of the blank periods of the display devices." (Emphasis Added)

Shelton fails to teach or disclose the features and limitations of "**receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process to make the CPU self-adjust a CPU clock rate and a power level of the CPU during a non-responding period of the CPU, wherein memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU**", "**executing the power saving process within a least common multiple occurrence of the blank periods of the display devices**", and "**a system memory directly accessed by the CPU**".

Examiner considers the graphic processing unit in Shelton as the CPU in claim 1 of the instant application; however, the graphic processing unit in claim 1 is not taught or disclosed after claim 1 is amended. Even though Examiner regards the graphic processing unit in Shelton as the graphic processing unit in claim 1, the CPU in the amended claim 1 is not taught by

Shelton. Since not all of the elements in amended claim 1 are disclosed or taught by Shelton in view of AAPA, claim 1 should be patentable over Shelton in view of AAPA.

Furthermore, the frame locking disclosed in Shelton is used to synchronize multiple graphic cards but not to execute the power saving process. Examiner stated "[C]learly, if Shelton's swap rate is lowered ...., then there will be a power saving ...." on page 21 of the detailed action. Applicants disagree on this statement of Examiner. In Shelton, in order to synchronize all of the graphic cards but not to save power, Shelton uses the lowest swap rate of the graphic card to synchronize all of the graphic cards. Using the lowest swap rate to synchronize all of the graphic cards is irrelevant to the power saving mechanism. Therefore, claim 1 of the instant application should be patentable over Shelton in view of AAPA.

Examiner further stated "[d]irect access can take place between a processor and a memory unit through an intermediate circuit". In the amended claim 1, it is clear that the memory controller is in the CPU, and the system memory is directly accessed by the CPU without any intermediate circuit. Moreover, Shelton fails to teach or disclose the connections of the frame buffer and the graphic card. Based on the foregoing differences, claim 1 should be patentable over Shelton.

In addition, Shelton fails to disclose the features **"memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU"**, **"executing the power saving process within a least common multiple occurrence of the blank periods of the display devices"**, and **"a system memory directly accessed by the CPU'**. In the amended claim 1, memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU. The power

saving process is then executed within a least common multiple occurrence of the blank periods of the display devices. Since Shelton lacks of disclosing the above features recited in claim 1, claim 1 should be patentable.

Claims 2-4 depend on claim 1. Since claim 1 is patentable, claims 2-4 are also patentable as matter of law.

Regarding claim 17, claim 17 is now recited as:

"A graphics display method for continuously displaying a plurality of graphics data on multiple display devices of a computer system that contains a central processing unit (CPU) which has a memory controller inside, a graphics-processing unit coupled to the memory controller, and **a system memory directly accessed by the CPU,** wherein the display devices are coupled to the graphics-processing unit, the method comprising:

providing a common clock source to the display devices and using the common clock source to synchronize blank periods of the display devices;

receiving a power saving signal from the CPU, the power saving signal indicates a request for executing a power saving process to make the CPU self-adjust a CPU clock rate and a power level of the CPU during a non-responding period of the CPU, wherein memory access from the graphics-processing unit to the system memory is blocked during the non-responding period of the CPU; and

executing the power saving process within a least common multiple occurrence of the blank periods of the display devices." (Emphasis Added)

The reasons of the patentability of claim 17 are same as those of claim 1, and therefore claim 17 should be patentable.

Claim 18 depends on claim 17. Since claim 17 is patentable, claim 18 is also patentable as matter of law.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-4 and 17-18 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
J.C. PATENTS

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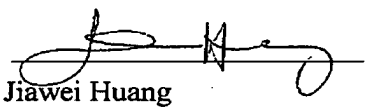

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